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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,937	08/05/2003	Joerg-Erich Sorg	12406-031001 / P2002	8847

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EXAMINER	
CHAMBLISS, ALONZO	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,937	SORG ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *1-20 and 41-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3, and 4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 21-40 in the reply filed on 12/21/04 is acknowledged.

2. Claims 1-20 and 41-45 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device claims, there being no allowable generic or linking claim.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 11/3/03, 3/15/04, and 11/23/04 was filed before the mailing date of the non-final rejection on 3/5/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is

suggested: " METHOD OF FABRICATING SURFACE MOUNTABLE SEMICONDUCTOR COMPONENTS WITH LEADFRAME STRIPS ".

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. In Claim 26, the phrase " light generating epitaxial layers " is vague and indefinite since it is not clear from the claim where the layers are located in the semiconductor component.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 21 –24, 27, and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuraishi et al. (WO 94/11902) in view of Kobayashi et al. (EP 1056126).

With respect to Claims 21-24, Kuraishi discloses applying an electrically insulating carrier layer 10 to an electrically conductive connection conductor layer 18, 20. Patterning at least one chip window 12 and at least one wire connection window 14 in the carrier layer 10 and patterning the external electrical connection conductors 18, 20 into the connection conductor layer. Mounting the semiconductor chip 24 into the chip window 14 and electrically connecting at least one electrical contact of the semiconductor chip 24 to a connection conductor 18 by means of a bonding wire 18b through the wire connection window 14. Placing the composite comprising patterned connection conductor layer 18, 20, patterned carrier layer 20, semiconductor chip 24, and bonding wire 18b into an injection mold. The semiconductor chip 24 including bonding wire 18b are encapsulated with an encapsulation material 26 by injection molding (see page 7 lines 1-37, page 9 lines 10-30, page 21 claims 15, 16, and page 22 claim17; Figs. 2D, 4,5A-5C, 7,12). Kuraishi does not explicitly disclose the encapsulating material that is subsequently at least partly cured and a mold having single cavity which spans all of the component regions of the array and forms a void

there essentially exclusively on the side of the semiconductor chips provided for the entire array. However, Kobayashi discloses an encapsulating material that is evident by Kobayashi. Kobayashi discloses an injection mold having a single cavity which spans all the component regions of the array and forms a void there essentially exclusively on the side of the semiconductor chips provided for the entire array (see col. 17 lines 35-45; Figs 3A, 3B, and 4). Thus, Kuraishi and Kobayashi have substantially the same environment of injection molding a semiconductor chip on a carrier. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate partly curing a resin in a single cavity with the process of Kuraishi, since the partly cured resin would prevent difficulty in handling the resin while preventing floating dust from entering the resin as taught by Kobayashi. Kuraishi discloses the claimed invention except for an array with a multiplicity of component regions with each case at least on chip window, wire connection window, and two external electrical connection conductors in a composite with a connection conductor layer and a carrier layer. Mounting a multiplicity of semiconductor chips into the chip windows and connecting electrical contacts of the chips to external electrical connections by means of multiplicity of bonding wires and encapsulating the chips. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an array with a multiplicity of component regions with each case at least on chip window, wire connection window, and two external electrical connection conductors in a composite with a connection conductor layer and a carrier layer. Mounting a multiplicity of semiconductor chips into the chip windows and connecting

electrical contacts of the chips to external electrical connections by means of multiplicity of bonding wires and encapsulating the chips, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

With respect to Claim 27, Kuraishi discloses the carrier layer consisting essentially of a plastic film (i.e. polyimide) and the connection conductor layer consisting essentially of a metal film (i.e. copper) (see page 7 lines 3-30).

With respect to Claims 30 and 31, Kuraishi discloses the connection conductor layer having a thickness of 60 micrometers (see page 9 lines 6-9).

With respect to Claim 32, Kuraishi discloses a first contact making window and a second contact making window are formed in the carrier layer, which windows lead to the first connection conductor and to the second connection conductor, respectively (see Figs. 4, 5A-5C, 7, and 12).

12. Claims 25, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuraishi et al. (WO 94/11902) and Kobayashi et al. (EP 1056126) as applied to claim 21 above, and further in view of Sano et al. (U.S. 6,486,543).

With respect to Claim 25, Kuraishi-Kobayashi discloses a semiconductor chip but fails to explicitly disclose the chip comprising a light emitting diode chip. It is well known in the semiconductor industry that a semiconductor chip includes a light emitting diode chip as evident by Sano (see col. 1 lines 14-18).

With respect to Claims 28 and 29, Kuraishi-Kobayashi discloses a carrier layer having a thickness. Kuraishi-Kobayashi fails to disclose a carrier layer having a

thickness of 60 micrometers. It is note that the specification contains no disclosure of either the critical nature of the claimed dimension or any unexpected results arising therefrom. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a carrier layer with a thickness of 60 micrometers into the process of Kuraishi-Kobayashi, since it has been held that where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16USPQ2d 1934, 1936 (Fed. Cir. 1990).

13. Claims 33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuraishi et al. (WO 94/11902) and Kobayashi et al. (EP 1056126) as applied to claim 21 above, and further in view of Fan et al. (U.S. 6,586,323).

With respect to Claims 33, 34, 39, and 40, Kuraishi-Kobayashi both fail to disclose a carrier layer comprises a plastic layer that can be patterned by means of masking and etching techniques. A portion of the plastic layer corresponding to at least the contact making window comprises an uncured and etchable plastic, and wherein the patterning step includes curing or incipiently curing the plastic layer except for a region of the plastic layer corresponding to at least the contact making window and subsequently removing the region that was not cured or incipiently cured. However, Fan discloses a carrier layer comprises a plastic layer (i.e. polyimide monomer) that can be patterned by means of masking and etching techniques. A portion of the plastic layer corresponding to at least the contact making window comprises an uncured and etchable plastic, and wherein the patterning step includes curing or incipiently curing the

plastic layer except for a region of the plastic layer corresponding to at least the contact making window and subsequently removing the region that was not cured or incipiently cured (see col. 1 lines 54-67, col. 5 lines 34-64, col. 6 lines 1-67, and col. 7 lines 1-50, and claim 1). Thus, Kuraishi-Kobayashi and Fan have substantially the same environment of a polyimide having a patterned with an opening. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate a masking and etching of the carrier layer of Kuraishi-Kobayashi, since the masking and etching of the carrier layer would remove the unwanted portion of the layer to expose a metal layer below as taught by Fan.

With respect to Claim 35 and 36, Fan discloses the patterning step includes applying a photoresist mask layer to the plastic layer, patterning or applying the mask layer in such a way that the region of the plastic layer is covered by the mask layer. Exposing the plastic layer and mask layer to radiation so that the plastic layer except for the region covered by the mask layer is incipiently cured or cured. The patterning step includes positioning a photomask above or on said plastic layer, the photomask shading the region of the plastic layer, exposing the plastic layer and photomask to radiation so that the plastic layer except for the region shaded by the photomask is cured or incipiently cured or cured, and lifting off the photomask layer (see col. 5 lines 45-67, col. 6 lines 1-67, and col. 7 lines 1-50, and claim 1).

With respect to Claim 37 and 38, Fan discloses the plastic layer that is cured by UV radiation which is thermal radiation (see col. 5 lines 50-60).

Allowable Subject Matter

14. Claim 26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach the combination of a light emitting diode chips are mounted onto the external electrical connections in rotated fashion with light generating epitaxial layers facing toward said connection in claim 26.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

15. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For

more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

AC/March 5, 2005

Alonzo Chambliss
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